Application for United States Letters Patent

for

Single-Ended to Differential Conversion Circuit with Duty Cycle Correction

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Field

[0001] The present invention relates to circuits, and more particularly, to analog circuits for providing a differential signal output in response to a single-ended signal input.

Background

[0002] In many computer systems, circuits utilize static logic CMOS (Complimentary Metal Oxide Semiconductor), where the signals of interest are single-ended signals. To increase speed and noise immunity, it may be desirable for high performance computer systems to employ current-mode logic circuits utilizing differential signaling. For example, in the simplified system of Fig. 1, die 102 and die 104 may communicate to each other via die 106, where die 102 and 104 may each comprise a microprocessor and die 106 comprises a switch. Switch 106 may also allow communication with cache 108, which is not on the same die as switch 106 or microprocessors 102 and 104. For speed and noise immunity, some or all of the signaling used for communication in the system of Fig. 1 may include differential signaling with current-mode transmission circuits, but many of the circuits in the microprocessors and switch may employ static logic CMOS. Furthermore, some of the circuits used within various functional unit blocks of a microprocessor may also employ current-mode logic CMOS. Consequently, it is desirable to interface single-ended signaling with differential signaling by providing a circuit that converts a single-ended signal into a differential signal.

[0003] A prior art single-ended to differential signal conversion circuit is illustrated in Fig. 2, where a single-ended voltage signal V_{IN} is applied at input port 202 and a differential voltage signal represented by the voltages V_{OUT+} and V_{OUT-} is taken at output ports 204 and 206, respectively. A reference voltage V_{REF} is applied at port 208, which may nominally be (Vcc-Vss)/2 where Vcc is the supply voltage and Vss is substrate (ground) voltage.

[0004] Ideally, it would be desirable for the circuit of Fig. 2 to have wide common-mode performance, that is, for the circuit performance to be the same for V_{IN} above V_{REF} as for V_{IN} below V_{REF}. However, in practice, the performance is different for V_{IN} in the range [Vss, (Vcc-Vss)/2] than for the range [(Vcc-Vss)/2, Vcc]. For example,

for V_{IN} close to Vss, pFET Q3 may go out of its saturation region as its drain-to-source voltage becomes small, in which case it will not act like a high (small-signal) impedance load to nFET Q1, but for V_{IN} in the range [(Vcc-Vss)/2, Vcc], pFET Q3 will present a high (small-signal) impedance load to nFET Q1, thereby resulting in a different amplifier gain for these two voltage regions.

Brief Description of the Drawings

[0005] Fig. 1 is a prior art computer system which may employ the embodiments of the present invention.

[0006] Fig. 2 is a prior art circuit for providing a differential signal output in response to a single-ended signal input.

[0007] Fig. 3 is an embodiment of the present invention.

Description of Embodiments

[0008] A circuit according to an embodiment of the present invention is illustrated in Fig. 3, where now reference to transistors Q*i*, where *i* is an integer from 1 to 14, now refers to transistors in Fig. 3. As for the circuit of Fig. 2, the circuit of Fig. 3 is a single-ended to differential signal conversion circuit, where a single-ended voltage signal V_{IN} is applied at input port 302 and a differential voltage signal represented by the voltages V_{OUT+} and V_{OUT-} is taken at output ports 304 and 306, respectively. A reference voltage V_{REF} is applied at port 308, which as for Fig. 2 may nominally be (Vcc-Vss)/2. However, the reference voltage V_{REF} may be adjusted to mitigate duty cycle distortion.

[0009] The amplifier comprising transistors Q9, Q10, Q11, and Q12 may be viewed as the complementary version of the amplifier comprising transistors Q1, Q2, Q3, and Q4. Consider first the amplifier comprising transistors Q1, Q2, Q3, and Q4, which for convenience will be labeled as amplifier An–. Transistors Q1 and Q2 comprise a nFET pair, and transistors Q3 and Q4 are configured as a current mirror. With the gate of transistor Q2 biased at a constant reference voltage V_{REF}, transistor Q3 serves as a current source to transistor Q1. With a slight abuse of notation, let An– also denote the small-signal voltage gain of amplifier An– when transistors Q9, Q10, Q11, and Q12 are not present. (It will be clear from context whether An– refers to a voltage gain or an amplifier.) It is readily seen that amplifier An– is a common-source amplifier. Applying a

simple, small-signal low-frequency model for the transistors in amplifier An– when in the active (saturation) region, such as the so-called T model, leads to an amplifier gain

$$An- = (-1)g_{m1}[r_{ds1} || r_{ds3}],$$

where g_{m1} is the small-signal transconductance of transistor Q1, r_{ds1} is the small-signal drain-source resistance of transistor Q1, and r_{ds3} is the small-signal drain-source resistance of transistor Q3. (For convenience, we shall use the notation that g_{mi} and r_{dsi} are the small-signal transconductance and resistance, respectively, of transistor Qi.)

[0010] Similarly, let Ap– denote the amplifier comprising transistors Q9, Q10, Q11, and Q12, as well as its small-signal voltage gain when amplifier An– is not present. The amplifier Ap– is also readily seen as a common-source amplifier. Again, using a simple low-frequency, small-signal active region model, its voltage gain is given by

$$Ap- = (-1)g_{m11}[r_{ds11} || r_{ds9}].$$

[0011] Now let A– denote the small-signal voltage gain of the amplifier comprising both amplifiers An– and Ap– as configured in Fig. 3. Modeling the transistors in these amplifiers as before leads to the voltage gain

$$A- = (-1)[g_{m1} + g_{m11}][r_{ds1} || r_{ds3} || r_{ds11} || r_{ds9}].$$

[0012] Now consider the amplifier comprising transistors Q5 through Q8, denoted as An+ in Fig. 3, where An+ also represents its voltage gain. Assuming both r_{ds6} and r_{ds8} are much greater than $1/g_{m8}$, a simple low-frequency, small-signal active region model yields

$$An+ = [(g_{m6})(g_{m7})/(g_{m8})][r_{ds5} || r_{ds7}].$$

The above expression for An+ could be written down by inspection by noting that amplifier An+ is similar to a common-source amplifier, except that the output port is taken at the drains of transistors Q5 and Q7, where the current mirror comprising transistors Q7 and Q8 mirrors the drain-source current of transistor Q6 to the small-signal loads provided by transistors Q5 and Q7. The voltage gain An+ is then seen to be simply the product of the transconductance of transistor Q6, g_{m6}, with the small-signal load provided by transistors Q7 and Q5, $[r_{ds5} || r_{ds7}]$, scaled by the mirror gain $(g_{m7})/(g_{m8})$.

[0013] Similarly, consider the amplifier comprising transistors Q13 through Q16, denoted as Ap+ in Fig. 3, where Ap+ also represents its small-signal voltage gain. This amplifier may be viewed as similar to a common-source amplifier, but with the current

mirror comprising transistors Q13 and Q14 mirroring the drain-source current of transistor Q16 to the loads provided by transistors Q13 and Q15. This voltage gain is easily seen to be

$$Ap+ = [(g_{m16})(g_{m13})/(g_{m14})][r_{ds13} || r_{ds15}].$$

[0014] Similar to the discussion regarding the combination of amplifiers An– and Ap–, if A+ represents the amplifier comprising the combination of amplifiers An+ and Ap+ with gain A+, it is easily seen that

$$A+ = [(g_{m6})(g_{m7})/(g_{m8}) + (g_{m16})(g_{m13})/(g_{m14})][r_{ds13} || r_{ds15} || r_{ds5} || r_{ds7}].$$

[0015] From the above expressions for A+ and A–, it follows that if $(g_{m1})(g_{m8}) = (g_{m6})(g_{m7})$; $(g_{m11})(g_{m14}) = (g_{m13})(g_{m16})$; $(r_{ds1} || r_{ds3}) = (r_{ds5} || r_{ds7})$; and $(r_{ds11} || r_{ds9}) = (r_{ds13} || r_{ds15})$, then

$$A+ = (-1)A-,$$

so that the circuit of Fig. 3 has the same small-signal voltage gain for V_{OUT+} as for V_{OUT-}. (The equality signs are interpreted to mean equality within the tolerances of the process technology.) Note that $(g_{m1})(g_{m8}) = (g_{m6})(g_{m7})$ is equivalent to $(g_{m1}) = (g_{m6})[(g_{m7})/(g_{m8})]$, which may be interpreted as setting the transconductance of transistor Q1 equal to the transconductance of transistor Q6 scaled by the gain of the current mirror comprising transistors Q7 and Q8. Similarly, $(g_{m11})(g_{m14}) = (g_{m13})(g_{m16})$ is equivalent to setting the transconductance of transistor Q11 equal to the transconductance of transistor Q16 scaled by the gain of the current mirror comprising transistors Q13 and Q14. Furthermore, the equalities $(r_{ds1} || r_{ds3}) = (r_{ds5} || r_{ds7})$ and $(r_{ds11} || r_{ds9}) = (r_{ds13} || r_{ds15})$ together may be interpreted as stating that the output ports 306 and 304 are loaded by equal amounts. These equalities may be satisfied in an embodiment for which transistors Q1, Q2, Q5, and Q6 are matched to each other; transistors Q3, Q4, Q7 and Q8 are matched to each other; transistors Q9, Q10, Q13, and Q14 are matched to each other; and transistors Q11, Q12, Q15, and Q16 are matched to each other. It is to be understood that transistors are matched if they have the same physical dimension and doping profile within the tolerances of the process technology. However, the circuit is not extremely sensitive to matching at the layout level because the input signal is full swing and thus device variation would have a small effect on the output signal.

[0016] It is interesting to note that under the assumption of modeling the transistors with a simple, low-frequency, small-signal, active region model, the small-signal voltage gain for the amplifier of Fig. 3 is not really improved over the smaller circuit consisting of only amplifiers An– and An+ or only amplifiers Ap– and Ap+. This follows by inspection of the above expressions for voltage gains. For example, it is not difficult to see that $|A-| \leq |An-| + |Ap-|$ and $|A+| \leq |An+| + |Ap+|$. As a more specific example, if the small-signal drain-source resistances are such that $r_{ds1} \| r_{ds3} = r_{ds11} \| r_{ds9}$, then it follows that $A- = (An- + Ap-)/2$, the arithmetic average of the voltage gains for amplifier An– and Ap–. Similarly, if the small-signal drain-source resistances are such that $r_{ds13} \| r_{ds15} = r_{ds5} \| r_{ds7}$, then it follows that $A+ = (An+ + Ap+)/2$, the arithmetic average of the voltage gains for amplifier An+ and Ap+.

[0017] The above expressions are only correct for the model used, which assumes that the transistors are in their active regions. However, for wide common-mode signals, a some transistors may go into their linear (or triode) regions, resulting in reduced performance. For example, suppose V_{IN} is near Vcc. Then nFETs Q1 and Q6 will go into their linear regions and will no longer be in their active (saturation) regions. In this case, the above expressions for amplification gain involving these nFETs are not correct. But, because the saturation region for pFETs is complementary to that of nFETs, amplifiers Ap– and Ap+ will still provide amplification because pFETs Q11 and Q16 will be in their active regions for V_{IN} near Vcc.

[0018] Similarly, suppose V_{IN} is near Vss. Then nFETs Q11 and Q16 will go into their linear regions and will no longer be in their active (saturation) regions. But, amplifiers An– and An+ will still provide amplification because pFETs Q1 and Q6 will be in their active regions for V_{IN} near Vss. Consequently, the complementary topology of the circuit of Fig. 3 exhibits, for the same technology, a wider common-mode region of operation than that of Fig. 2. In this way, the circuit of Fig. 3 provides a full-swing differential output in response to a full-swing single-ended input.

[0019] Various modifications may be made to the disclosed embodiment without departing from the scope of the invention as claimed below. For example, other types of current mirrors may be employed to provide a higher small-signal load impedance,

resulting in a tradeoff between bandwidth and amplifier gain. The particular embodiment of Fig. 3 has been found to operate at a clock frequency as high as 10GHz.

[0020] It is to be understood in these letters patent that the meaning of "*A* is connected to *B*" is that *A* and *B* are connected by a passive structure for making a direct electrical connection so that the voltage potentials of *A* and *B* are substantially equal to each other. For example, *A* and *B* may be connected by way of an interconnect, transmission line, etc. In integrated circuit technology, the "interconnect" may be exceedingly short, comparable to the device dimension itself. For example, the gates of two transistors may be connected to each other by polysilicon or copper interconnect that is comparable to the gate length of the transistors.

[0021] It is also to be understood that the meaning of "*A* is coupled to *B*" is that either *A* and *B* are connected to each other as described above, or that, although *A* and *B* may not be connected to each other as described above, there is nevertheless a device or circuit that is connected to both *A* and *B*. This device or circuit may include active or passive circuit elements. For example, *A* may be connected to a circuit element which in turn is connected to *B*.

[0022] It is also to be understood in these letters patent that a "current source" may mean either a current source or a current sink. Similar remarks apply to similar phrases, such as, "to source current".

[0023] It is also to be understood that various circuit blocks, such as current mirrors, amplifiers, etc., may include switches so as to be switched in or out of a larger circuit, and yet such circuit blocks may still be considered connected to the larger circuit because the various switches may be considered as included in the circuit block.

[0024] It is also to be understood that a claimed equality or match is interpreted to mean an equality or match within the tolerances of the process technology.